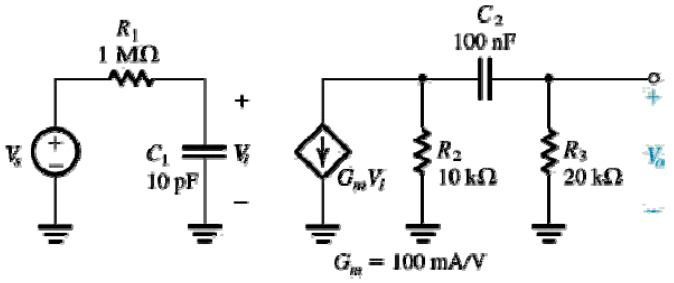
國立高雄大學 101 學年度博士班招生考試試題

科目：電子學　　系所組別：電機工程學系　　是否使用計算機：是
考試時間：100 分鐘　　本科原始成績：100 分

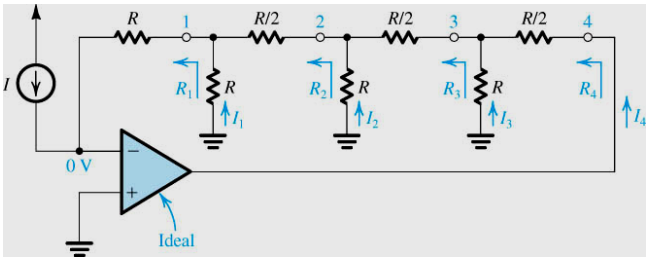
1. (15%) For the circuit shown in Fig. 1 first, evaluate $T_i(s)=V_i(s)/V_s(s)$ and the corresponding cutoff (corner) frequency. Second, evaluate $T_o(s)=V_o(s)/V_i(s)$ and the corresponding cutoff frequency. Put each of the transfer functions in the standard form and combine them to form the overall transfer function, $T(s)=T_i(s)\times T_o(s)$. Provide a Bode magnitude plot for $|T(jw)|$. What is the bandwidth between 3-dB cutoff points?

Fig. 1



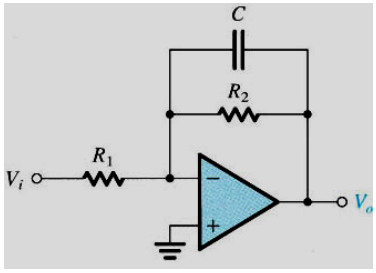
2. (15%) The circuit is shown in Fig.2.
   (a) Find the resistances looking into node 1, R_1; node 2, R_2; node 3, R_3; and node 4, R_4.
   (b) Find the current I_1, I_2, I_3, and I_4 in terms of the input current I.
   (c) Find the voltages at nodes 1, 2, 3, and 4, that is V_1, V_2, V_3, and V_4 in terms of (IR).

Fig. 2



3. (15%) Fig. 3 shows a circuit that performs a low-pass STC function. Such a circuit is known as a first-order low-pass active filter. Derive the transfer function, the dc gain and the 3-dB frequency. Design the circuit to obtain an input resistance of 1kΩ, a dc gain of 20dB, and a 3dB frequency of 4kHz. At what frequency does the magnitude of the transfer function reduce to unity?

Fig. 3



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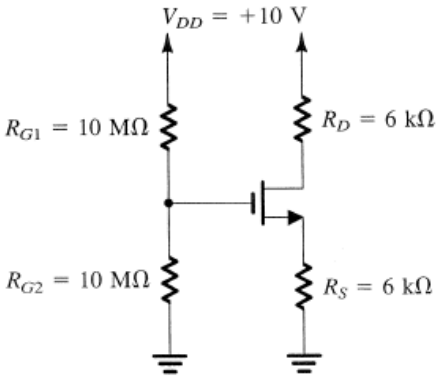
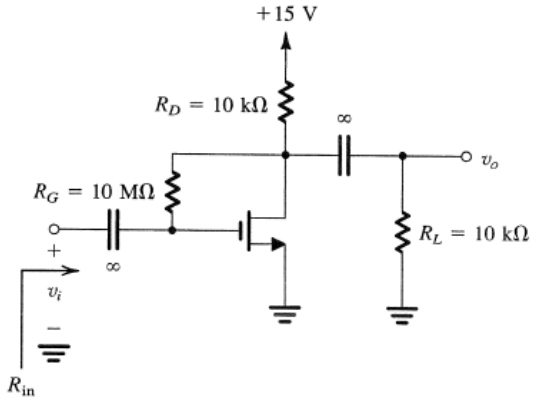
4. (10%) Analyze the circuit shown in Fig. 4 to determine the voltages at all nodes and the currents through all branches. Let V_t = 1V and $k'_n(W/L)$ = 1 mA/V^2. Neglect the channel-length modulation effect (i.e., assume λ=0). (10%)

Fig. 4



5. (20%) Fig. 5 shows a discrete common-source MOSFET amplifier utilizing the drain-to-gate feedback biasing arrangement. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has V_t = 1.5 V, $k'_n(W/L)$ = 0.25 mA/V^2, and V_A = 50 V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.

Fig. 5



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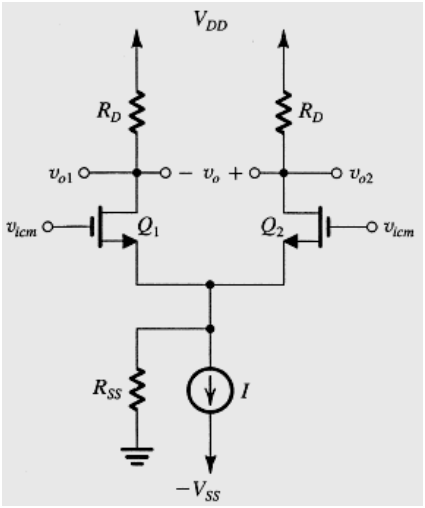
6. (15%) A MOS differential pair operated at a bias current of 0.8mA employs transistors with $W/L=100$ and $\mu_n C_{ox}$=0.2mA/V^2, using R_D=5kΩ, and R_{SS}=25 kΩ, as shown in Fig. 6.
   (a) Find the differential gain, the common-mode gain, and the common-mode rejection ratio (in dB) if the output is taken single-endedly and the circuit is perfectly matched.
   (b) Repeat (a) when the output is taken differentially.
   (c) Repeat (a) when the output is taken differentially but the drain resistances have a 1% mismatch.

Fig. 6



7. (10%) Sketch a CMOS logic circuit that realizes the Boolean function $Y = \overline{A + B \bullet (C+D)}$.

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科目：計算機概論　　系所組別：電機工程學系　　是否使用計算機：是
考試時間：100 分鐘　　本科原始成績：100 分

1. Please explain “NP-completeness (NPC)” and give several NPC problems. (25%)
2. What is 3D IC? What are the compacts that 3D IC may bring to the IT industry? (25%)
3. What is “Quantum Computing”? What the computer organization may be in a quantum computing age? (25%)
4. Recently, major CPU manufacturers announce new APU (Accelerated Processing Unit) products to the market for the next-generation computers. Please state what an APU is and why it is the emerging trend of future computers. (25%)